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A practical FPGA reference that's like an on-call mentor for engineers and computer scientists. Addressing advanced issues of FPGA (Field-Programmable Gate Array) design and implementation, Advanced FPGA Design: Architecture, Implementation, and Optimization accelerates the learning process for engineers and computer scientists. With an emphasis on real-world design and a logical, practical approach, it walks readers through specific challenges and significantly reduces the learning curve.

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Advanced FPGA design: Architecture, Implementation, and Optimization/ by Steve Kilts. p. cm. Includes index. ISBN 978-0-470-05437-6 (cloth) 1. Field programmable gate arrays- -Design and construction. I. Title. TK7895.G36K55 2007 621.3905- -dc22 2006033573 Printed in the United States of America 10 98 76 54 3 21

Advanced FPGA Design - pudn.com

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that ...

Advanced FPGA Design: Architecture, Implementation, and ...

Advanced FPGA Design 作者 : Steve Kilts 出版社: Wiley-IEEE Press 副标题: Architecture, Implementation, and Optimization 出版年: 2007-06-29 页数: 352 定价: USD 112.00 装帧: Hardcover ISBN: 9780470054376

Advanced FPGA Design (豆瓣)

Advanced Fpga Design : Architecture, Implementation, and Optimization, Hardcover by Kilts, Steve, ISBN 0470054379, ISBN-13 9780470054376, Brand New, Free shipping in the US A consulting engineer based in Minnesota, Kilts consolidates years of his white papers and application notes for specific projects into a broad guide to help designers become advanced designers of field programmable gate arrays.

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Advanced FPGA Design

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Advanced FPGA Design by Kilts, Steve (ebook)

This paper presents design, implementation and comparison of highly efficient architectures for AES on FPGAs: Iterative architecture and pipelined architecture. The first design is optimized for area and the second one is optimized for speed.

Efficient Hardware Architectures for AES on FPGA ...

inference accuracy. An FPGA implementation is used as the validation vehicle for our design, achieving a 2.28ms inference latency for the ImageNet benchmark. Our implementation shines in that it has 9x higher energy efficiency compared to other implementations while achieving comparable latency. A highlight of our approach

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